

Features

- OSFP MSA 5.0 and CMIS 5.1 compliant
- Duplex LC connector
- 8x53.125Gb/s electrical interface (400GAUI-8)
- 4x106.25Gbps optical interface
- Up to 2km over SMF
- Power dissipation $\leq 9W$
- Operating case temperature: 0°C to 70°C
- IEEE 802.3cu compliant
- Built-in digital diagnostic functions
- 3.3V power supply voltage
- RoHS compliant



Application

- 400GBASE-FR4 Ethernet
- Data center networks
- InfiniBand NDR applications

Ordering Information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX	Sen (dBm)	Temp (°C)	Reach (KM)	DDM
ELOM400G-OSFP-FR4-S	OSFP	400G	CWDM EML	-3.2~4.4	PIN	<-6	0~70	2	Y

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	-0.5	3.6	V
Storage Temperature	T _{sto}	-40	85	°C
Relative Humidity (Non- condensing)	RH	5	95	%
Control Input Voltage	V _i	-0.3	V _{CC} +0.5	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V
Case Operating Temperature	T _{op}	0		70	°C
Relative Humidity (Non- condensing)	RH	15		85	%
Distance 9/ 125um G.652 SMF	D		2		KM

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Power Supply Current	I _{cc}			2875	mA
Power On Initialization Time	T _{init}			2000	ms
Transmitter					
Signaling Speed, each lane			53.125		GBd
Center wavelength	L0	1264.5	1271	1277.5	nm
	L1	1284.5	1291	1297.5	nm
	L2	1304.5	1311	1317.5	nm
	L3	1324.5	1331	1337.5	nm
Signaling Speed Tolerance		-100		+100	ppm
Differential pk-pk input voltage tolerance	V _{in,pp}	750			mV
AC common-mode RMS voltage tolerance		25			mV
Differential Input Impedance	Z _{in}	90	100	110	Ohms
Effective return loss	ERL	8.5			dB
Single-ended voltage tolerance range		-0.4		303	V
DC Common Mode Voltage		-0.35		2.85	V
Receiver					
Signaling Speed, each lane			53.125		GBd
Signaling Speed Tolerance		-100		+100	ppm
Differential pk-pk output voltage	V _{out,pp}			600	mV

Short mode				845	
Long mode					
Eye Height	EH			15	mV
Differential Input Impedance	Z_{out}	90	100	110	Ohms
Transition Time, 20% to 80%	T_r, T_f	8.5			ps
DC Common Mode Voltage		-0.35		2.85	V
AC Common Mode output Voltage (RMS)		25			mV

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Signaling Speed			53.125		GBd	1
Signaling Speed Tolerance		-100		+100	ppm	
Modulation Format		PAM4				
Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average TX Power	P_{avg}	-3.2		4.4	dBm	1
Outer Optical Modulation Amplitude for TDECQ < 1.4dB For 1.4dB ≤ TDECQ ≤ 3.4dB	OMA_{outer}	-1.1- 0.3+TDECQ		3.7	dBm	1,2
Extinction Ratio	ER	3.5			dB	1
Avg Launch Power TX Off	P_{off}			-16	dBm	1
Transmitter & Dispersion Eye Closure	TDECQ			3.4	dB	1
Transmitter eye closure	TECQ			3.4	dB	1
TDECQ - TECQ				2.5	dB	
Transmitter transition time				17	ps	
Relative Intensity Noise	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORLT			15.6	dB	
Reflectance				-26	dB	
Receiver						
Signaling Speed			53.125		GBd	1
Signaling Speed Tolerance		-100		+100	ppm	

Modulation Format		PAM4				
Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Damage Threshold		5			dBm	1
Average RX Power		-8.2		4.4	dBm	1
RX Power (OMA _{outer})				4.5	dBm	
RX Reflectance				-26	dBm	
RX Sensitivity (OMA _{outer}) for TECQ < 1.4dB for 1.4dB ≤ TECQ ≤ 3.4dB	Sen- OMA			-4.6 - 6.0+TE CQ	dBm	3
Stressed RX Sensitivity (OMA _{outer})				-4.1	dBm	1
Conditions of Stressed RX Sensitivity Test						
Stressed Eye Closure, lane under test	SECQ	3.4			dB	
OMA _{outer} of Each Aggressor Lane		/			dBm	

Optical Characteristics

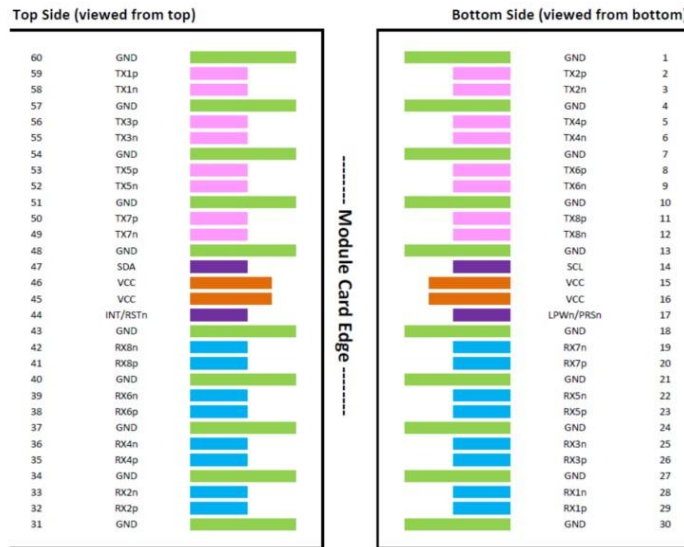
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Signaling Speed			53.125		GBd	1
Signaling Speed Tolerance		-100		+100	ppm	
Modulation Format		PAM4				
Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average TX Power	P _{avg}	-3.2		4.4	dBm	1
Outer Optical Modulation Amplitude for TDECQ < 1.4dB For 1.4dB ≤ TDECQ ≤ 3.4dB	OMA _{outer}	-1.1- 0.3+TDECQ		3.7	dBm	1,2
Extinction Ratio	ER	3.5			dB	1
Avg Launch Power TX Off	P _{off}			-16	dBm	1
Transmitter & Dispersion Eye Closure	TDECQ			3.4	dB	1

Transmitter eye closure	TECQ			3.4	dB	1
TDECQ - TECQ				2.5	dB	
Transmitter transition time				17	ps	
Relative Intensity Noise	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORLT			15.6	dB	
Reflectance				-26	dB	
Receiver						
Signaling Speed			53.125		GBd	1
Signaling Speed Tolerance		-100		+100	ppm	
Modulation Format		PAM4				
Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Damage Threshold		5			dBm	1
Average RX Power		-8.2		4.4	dBm	1
RX Power (OMAouter)				4.5	dBm	
RX Reflectance				-26	dBm	
RX Sensitivity (OMAouter) for TECQ < 1.4dB for 1.4dB ≤ TECQ ≤ 3.4dB	Sen- OMA			-4.6 - 6.0+TE CQ	dBm	3
Stressed RX Sensitivity (OMAouter)				-4.1	dBm	1
Conditions of Stressed RX Sensitivity Test						
Stressed Eye Closure, lane under test	SECQ	3.4			dB	
OMAouter of Each Aggressor Lane		/			dBm	

Notes:

- Each lane.
- For 400GBASE-DR4 the requirement on the OMAouter(min) applies even in the cases where TDECQ<1.4dB.
- Measured with conformance test signal at TP3 for BER=2.4x10⁻⁴.

Pin Definition

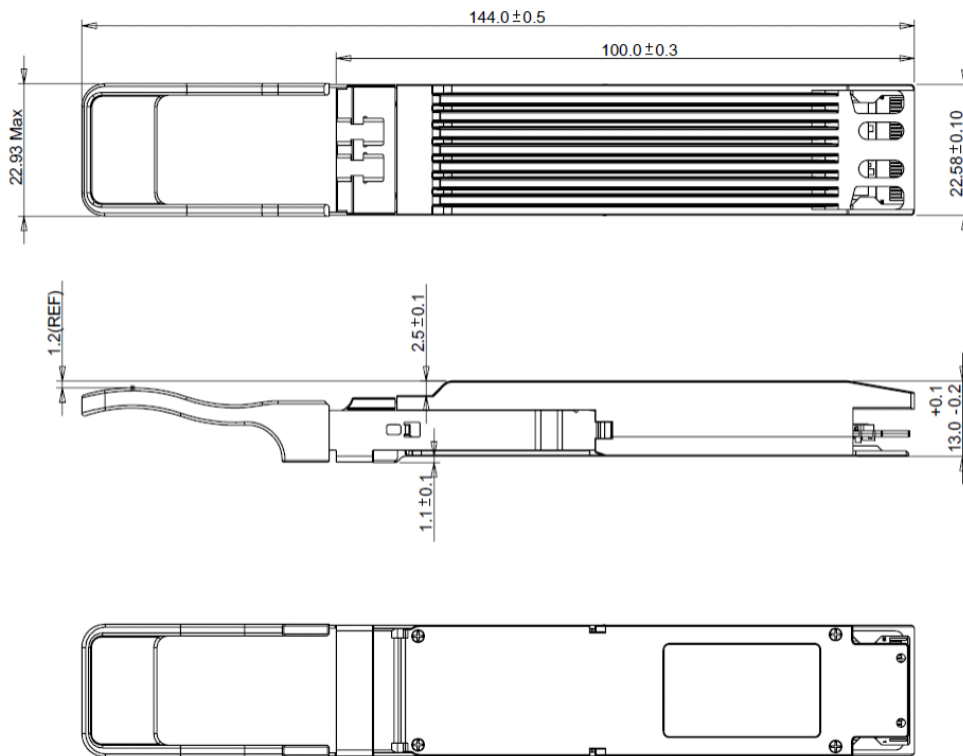


Pin	Logic	Symbol	Description	Notes
1		GND	Ground	
2	CML-I	TX2p	Transmitter Data Non-Inverted	
3	CML-I	TX2n	Transmitter Data Inverted	
4		GND	Ground	
5	CML-I	TX4p	Transmitter Data Non-Inverted	
6	CML-I	TX4n	Transmitter Data Inverted	
7		GND	Ground	
8	CML-I	TX6p	Transmitter Data Non-Inverted	
9	CML-I	TX6n	Transmitter Data Inverted	
10		GND	Ground	
11	CML-I	TX8p	Transmitter Data Non-Inverted	
12	CML-I	TX8n	Transmitter Data Inverted	
13		GND	Ground	
14	LVC MOS-I/O	SCL	2-wire Serial interface clock	Open-Drain with pull up resistor on Host
15	Power from Host	VCC	+3.3V Power	
16	Power from Host	VCC	Ground +3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	See pin description for required circuit

18		GND	Ground	
19	CML-O	RX7n	Receiver Data Inverted	
20	CML-O	RX7p	Receiver Data Non-Inverted	
21		GND	Ground	
22	CML-O	RX5n	Receiver Data Inverted	
23	CML-O	RX5p	Receiver Data Non-Inverted	
24		GND	Ground	
25	CML-O	RX3n	Receiver Data Inverted	
26	CML-O	RX3p	Receiver Data Non-Inverted	
27		GND	Ground	
28	CML-O	RX1n	Receiver Data Inverted	
29	CML-O	RX1p	Receiver Data Non-Inverted	
30		GND	Ground	
31		GND	Ground	
32	CML-O	RX2p	Receiver Data Non-Inverted	
33	CML-O	RX2n	Receiver Data Inverted	
34		GND	Ground	
35	CML-O	RX4p	Receiver Data Non-Inverted	
36	CML-O	RX4n	Receiver Data Inverted	
37		GND	Ground	
38	CML-O	RX6p	Receiver Data Non-Inverted	
39	CML-O	RX6n	Receiver Data Inverted	
40		GND	Ground	
41	CML-O	RX8p	Receiver Data Non-Inverted	
42	CML-O	RX8n	Receiver Data Inverted	
43		GND	Ground	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	See pin description for required circuit
45	Power from Host	VCC	+3.3V Power	
46	Power from Host	VCC	+3.3V Power	
47	LVC MOS-I/O	SDA	2-wire Serial interface data	Open-Drain with pull up resistor on Host
48		GND	Ground	
49	CML-I	TX7n	Transmitter Data Inverted	

50	CML-I	TX7p	Transmitter Data Non-Inverted	
51		GND	Ground	
52	CML-I	TX5n	Transmitter Data Inverted	
53	CML-I	TX5p	Transmitter Data Non-Inverted	
54		GND	Ground	
55	CML-I	TX3n	Transmitter Data Inverted	
56	CML-I	TX3p	Transmitter Data Non-Inverted	
57		GND	Ground	
58	CML-I	TX1n	Transmitter Data Inverted	
59	CML-I	TX1p	Transmitter Data Non-Inverted	
60		GND	Ground	

Package Outline



Label Information

